Claims

1. A method for forming an integrated circuit comprising the steps of:

providing a semiconductor substrate having a perimeter;

forming a layer of material overlying the semiconductor substrate;

providing a polishing pad having a center and a perimeter, the polishing pad having a tapered region that extends from the perimeter of the polishing pad to a selected location offset from the center of the polishing pad; and

polishing the layer of material, wherein during polishing the perimeter of the semiconductor substrate overlies the tapered region of the polishing pad for a selected period of time.

2. The method of claim 1, further comprising the step of moving the substrate radially across the polishing pad while polishing the layer of material.

3. The method of claim 1, wherein the polishing pad has a first thickness at the selected location and a second thickness at the perimeter, and wherein the second thickness is less than the first thickness.

4. The method of claim 1, wherein the layer of material is further characterized as a copper layer.

5. The method of claim 4, further comprising the step of dispensing a slurry comprising hydrogen peroxide on the polishing pad.

6. The method of claim 1, wherein the layer of material is further characterized as a tungsten layer.

7. The method of claim 6, further comprising the step of dispensing a slurry comprising ferric nitrate on the polishing pad.

8. The method of claim 1, wherein the layer of material is further characterized as a silicon oxide layer.

9. The method of claim 8, further comprising the step of dispensing a slurry comprising potassium hydroxide on the polishing pad.

10. The method of claim 1, wherein the tapered region is further characterized as having a constant angle taper.

11. The method of claim 1, wherein the tapered region is further characterized as having a variable angle taper.

12. A method for forming an integrated circuit comprising the steps of:

providing a semiconductor substrate having a center and an edge region;

forming a layer of material overlying the semiconductor substrate;

providing a polishing pad having a central region, a perimeter, and a peripheral region lying between the perimeter and the central region; the central region having a first front surface and the peripheral region having a second front surface, wherein the second front surface lies below the first front surface; and

polishing the layer of material, wherein during polishing only the edge region of the semiconductor substrate is allowed to overlie the second front surface.

13. The method of claim 12, further comprising the step of moving the substrate radially across the polishing pad while polishing the layer of material.

14. The method of claim 12, wherein the layer of material is further characterized as a copper layer.

15. The method of claim 12, wherein the layer of material is further characterized as a tungsten layer.

16. The method of claim 12, wherein the layer of material is further characterized as a silicon oxide layer.

17. The method of claim 12, wherein the peripheral region comprises a horizontal region.

18. The method of claim 12, wherein the peripheral region comprises a tapered region.

19. The method of claim 12, wherein the peripheral region comprises a substantially vertical sidewall.

20. The method of claim 12, wherein the peripheral region comprises a grooved region.

21. The method of claim 12, further comprising the step of providing a polishing platen having a tapered region, wherein the peripheral region of the polishing pad conforms to the tapered region of the polishing platen.

22. A method for forming an integrated circuit comprising the steps of:

providing a semiconductor substrate having a center and an edge region;

forming a layer of material overlying the semiconductor substrate;

providing a polishing pad having a central region, a perimeter, and a peripheral region lying between the perimeter and the central region; the central region having a first front surface and the peripheral region having a second front surface, wherein a portion of the second front surface lies below the first front surface; and

polishing the layer of material, wherein during polishing only the edge region of the semiconductor substrate is allowed to overlie the portion of the second front surface.

23. The method of claim 22, further comprising the step of moving the substrate radially across the polishing pad while polishing the layer of material.

24. The method of claim 22, wherein the layer of material is further characterized as a copper layer.

25. The method of claim 22, wherein the layer of material is further characterized as a tungsten layer.

26. The method of claim 22, wherein the layer of material is further characterized as a silicon oxide layer.

27. The method of claim 22, wherein the peripheral region comprises a horizontal region.

28. The method of claim 22, wherein the peripheral region comprises a tapered region.

30. The method of claim 22, wherein the peripheral region comprises a grooved region.

31. The method of claim 30, wherein the grooved region is further characterized as being U-shaped.

32. The method of claim 30, wherein the grooved region is further characterized as being V-shaped.

33. A polishing apparatus comprising:
a polishing platen;
a polishing pad overlying the polishing pad, the polishing pad having a central region and a peripheral region, the central region having a first front surface and the peripheral region having a second front surface, wherein at least a portion of the second front surface lies below the first front surface; and
a carrier overlying the polishing pad.

34. The apparatus of claim 33, wherein the polishing platen is further characterized as having a tapered region, and wherein the peripheral region of the polishing pad overlies the tapered region.

35. The apparatus of claim 22, wherein the peripheral region comprises a horizontal region.

36. The apparatus of claim 22, wherein the peripheral region comprises a tapered region.

37. The apparatus of claim 22, wherein the peripheral region comprises a grooved region.

38. The apparatus of claim 37, wherein the grooved region is further characterized as being U-shaped.

39. The apparatus of claim 37, wherein the grooved region is further characterized as being V-shaped.